What is claimed is:

1. A method of forming sidewall spacers adjacent opposing vertical sides of a gate electrode, comprising:

forming at least one gate electrode over a substrate;

forming a first silicon oxide film conformally over the substrate and gate electrode from a combination of gases including bis-(tertiarybutylamino)silane and oxygen;

forming a silicon nitride film conformally over the first silicon oxide film from a combination of gases including bis-(tertiarybutylamino)silane; and

forming a second silicon oxide film over the silicon nitride film from a combination of gases including bis-(tertiarybutylamino)silane and oxygen.

2. The method of Claim 1, wherein forming the first silicon oxide film comprises providing one or more wafers in a furnace at a first temperature, and flowing BTBAS and oxygen into the furnace.

3. The method of Claim 2, wherein, forming the silicon nitride film, and the second silicon oxide film comprises keeping the one or more wafers in the furnace.

4. The method of Claim 2, wherein forming the silicon nitride film comprises maintaining the one or more wafers in the furnace at a second temperature, and flowing BTBAS and NH_3 into the furnace.

5. The method of Claim 4, wherein forming the second oxide film comprises maintaining the one or more wafers in the furnace at the first temperature and flowing BTBAS and oxygen into the furnace.

6. The method of Claim 4, wherein the first temperature is in the range of 550°C to 580°C, and the second temperature is in the range of 580°C to 600°C.

7. The method of Claim 1, further comprising, prior to forming the film silicon nitride film and subsequent to forming the first oxide film, purging the furnace.

8. The method of Claim 7, wherein purging the furnace comprises ceasing the flow of BTBAS and oxygen, and flowing N_2 into the furnace.

9. The method of Claim 1, further comprising, prior to forming the second oxide film and subsequent to forming the silicon nitride film, purging the furnace.

10. The method of Claim 9, wherein purging the furnace comprises ceasing the flow of BTBAS and NH_3, and flowing N_2 into the furnace.

11. A method of forming a transistor, comprising:

forming at least one gate electrode over a gate dielectric layer, the gate dielectric layer disposed on a substrate;

depositing a first silicon oxide film conformally over the substrate and gate electrode from a combination of gases comprising bis-(tertiarybutylamino)silane and oxygen;

depositing a silicon nitride film conformally over the first silicon oxide film from a combination of gases comprising bis-(tertiarybutylamino)silane and ammonia;

depositing a second silicon oxide film over the silicon nitride film from a combination of gases comprising bis-(tertiarybutylamino)silane and oxygen; and

forming a first sidewall spacer.

12. The method of Claim 11, wherein the first silicon oxide, the silicon nitride, and the second silicon oxide are deposited in-situ.

13. The method of Claim 11, wherein depositing the first silicon oxide, the silicon nitride, and the second silicon oxide are all done in a first furnace.

14. The method of Claim 13, wherein the first furnace is vertically oriented and the BTBAS, oxygen, nitrogen, and ammonia, each flow into the furnace from a bottom of the vertically oriented furnace.

15. The method of Claim 11, further comprising implanting dopants to form a of deep source/drain region in the substrate adjacent at least two opposing sides of the gate electrode.

16. The method of Claim 14, wherein forming a first sidewall spacer comprises anisotropically etching the second silicon oxide layer, the silicon nitride layer, and the first silicon oxide layer.

17. The method of Claim 16, further comprising removing the second oxide layer so as to form L-shaped spacers.

18. The method of Claim 17, further comprising implanting dopants to form a deep source/drain region in the substrate, adjacent to each opposing side of the L-shaped spacers.

19. The method of Claim 17, wherein implanting dopants includes a partial passage of ions from an ion beam through a portion of the L-shaped spacers.

20. A field effect transistor, comprising:

a gate electrode overlying a gate dielectric layer disposed on a substrate;

a pair of L-shaped spacers adjacent opposing vertical sidewalls of the gate electrode; and

a pair of source/drain regions disposed in the substrate and aligned, respectively, adjacent to the pair of L-shaped spacers;

wherein each of the source/drain regions has a shallow tip portion underlying each L-shaped spacer, a deep portion spaced away from the L-shaped spacer, and an intermediate portion having a depth greater than that of the shallow tip portion and less than that of the deep portion.

21. The field effect transistor of Claim 20, wherein each L-shaped spacer comprises a silicon oxide layer immediately adjacent to the gate electrode.

22. The field effect transistor of Claim 21, wherein each L-shaped spacer comprises a silicon nitride layer adjacent to the silicon oxide layer.

23. The field effect transistor of Claim 22, wherein the silicon nitride layer is thicker than the silicon oxide layer.